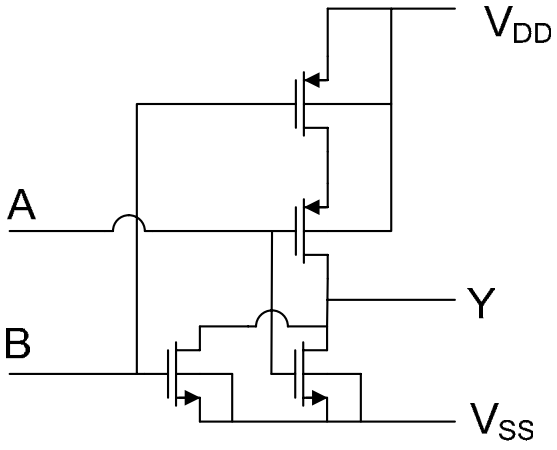
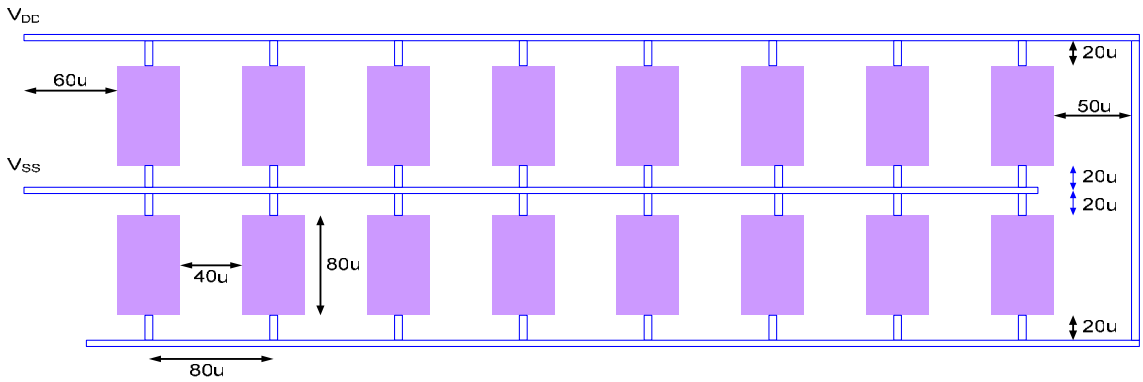
EE 434
Homework Assignment 3
Fall 2006

Problem 1 Provide a layout of the following circuit with the goal of minimizing the total area of a square enclosing the layout of the circuit. Use the AMI 0.5u CMOS process. All electrical connections should exit the layout in Metal 1 and there should be no DRC violations. What is the overhead factor (Total circuit area divided by gate area) for your circuit? Your score for this problem will be based upon how small of a total area you achieve without violating any design rules.



$W_n = 16\lambda \quad W_p = 32\lambda$
$L_n = L_p = 2\lambda$

Problem 2 A Metal-1 interconnect (shown in blue) for a circuit is shown. Assume it is to drive loads (purple shaded) that can be modeled as 200 ohm resistors. Ideally this metal interconnect is to provide 5V across each element for the entire circuit but due to ohmic drops in the metal interconnect, there is some degradation in voltage. What is the minimum voltage actually delivered to each of the blocks? Key dimensions are given for everything except the metal width which is 4u. Resize the metal interconnect so that the minimum voltage supplied to any of the loads is 4.9V. (Use the AMI 0.5u process)


VDD
60u
VSS
20u
50u
20u
20u
40u
80u
20u
80u